CLAIMS:

1. A method for writing to NV memories in a controller architecture, characterized in that (a) defined data value(s) or (a) defined data word(s) is/are written to (a) defined destination address(es) within the NV memory, by writing the data value(s) or the data word(s) to the predetermined position of the cache page register of the NV memory and updating the page address pointer registers of the NV memory.

2. A method as claimed in claim 1, characterized in that, for writing to the NV memory, the instruction set of the controller core is extended by additional move code write instructions (MOVCWR instructions).

3. A method as claimed in one of the preceding claims, characterized in that the additional instructions of the controller core perform a transfer of the parameters for address pointers and for the data value to be written or the data word to be written and activate corresponding control signals for a memory management unit (MMU) and NV memory interfaces.

4. A method as claimed in one of the preceding claims, characterized in that the address processing for the MOVCWR instructions is performed in the same way as the processing of code fetches or MOVC instructions, in the presence of a memory management unit (MMU).

5. A method as claimed in one of the preceding claims, characterized in that this MMU is extended by a control signal path in the presence of a memory management unit (MMU) of the controller.

6. A method as claimed in one of the preceding claims, characterized in that, in the presence of an MMU, only address areas of the NV memory are written to which have been enabled by the MMU.

7. A method as claimed in one of the preceding claims, characterized in that special mapping of the code memory is taken into account within the address area of the controller in the presence of an MMU.

8. A method as claimed in one of the preceding claims, characterized in that a plurality of data values and/or data words with the same page address are written in succession.

9. A method as claimed in one of the preceding claims, characterized in that the content of the cache page register is programmed into the NV memory by writing to the control register of the NV memory.

10. A method as claimed in one of the preceding claims, characterized in that the cache page register of the NV memory is cleared when changing to a new page address in the event of an MOVCWR instruction.

11. A method as claimed in one of the preceding claims, characterized in that undesired programming of old page register contents under incorrect addresses is prevented.

12. An arrangement having a processor, which is designed in such a way that writing to NV memories in a controller architecture may be performed, wherein (a) defined data value(s) or (a) defined data word(s) is/are written to (a) defined destination address(es) within the NV memory, by writing the data value(s) or the data word(s) to the predetermined position of the cache page register of the NV memory and updating the page address pointer registers of the NV memory.

13. An arrangement having a processor as claimed in claim 12, characterized in that the processor is part of a smart card controller and the arrangement is a smart card.

14. A computer program product which comprises a computer-readable storage medium, on which a program is stored which, once it has been loaded into the memory of a computer or of a smart card controller, allows the computer or smart card controller to perform writing to NV memories in a controller architecture, wherein (a) defined data value(s) or (a) defined data word(s) is/are written to (a) defined destination address(es) within

the NV memory, by writing the data value(s) or the data word(s) to the predetermined position of the cache page register of the NV memory and updating the page address pointer registers of the NV memory.

15. A computer-readable storage medium, on which a program is stored which, once it has been loaded into the memory of a computer or of a smart card controller, allows the computer or smart card controller to perform writing to NV memories in a controller architecture, wherein (a) defined data value(s) or (a) defined data word(s) is/are written to (a) defined destination address(es) within the NV memory, by writing the data value(s) or the data word(s) to the predetermined position of the cache page register of the NV memory and updating the page address pointer registers of the NV memory.